a plurality of pieces of compliant adhesive film interposed between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer.

39. The semiconductor device package of claim 38 wherein the pieces of compliant adhesive film comprise an elastomer material.

40. The semiconductor device package of claim 38 wherein the pieces of compliant adhesive film comprise strips of compliant adhesive material positioned in parallel with a longitude of the semiconductor die.

17 41. The semiconductor device package of claim 15 38, further comprising an external conductive terminal electrically coupled to the electrically conductive interconnect and positioned on a surface of the interposer opposite of the die attach surface.

42. A semiconductor device package, comprising:

a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die; and

a plurality of strips of adhesive film interposed between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer.

43. The semiconductor device package of claim 42 wherein the strips of adhesive film are positioned substantially parallel with a longitude of the semiconductor die.

21 44. The semiconductor device package of claim 19 42 wherein a first and a second strip of the plurality are positioned substantially at a right angle with respect to each other.

to adhere a semiconductor die to an interposer to reduce failures caused by shearing forces resulting from unmatched thermal expansion rates of the interposer and the semiconductor die. As described in the specification, the cumulative thermal expansion for the multiple pieces of adhesive film is less than the thermal expansion for a single layer of elastomer material. Stress on wire bond joints resulting from the different coefficients of thermal expansion between the die and the substrate are consequently reduced.

The package assembly described in the Khandros patent includes a flexible interposer having an upper layer upon which conductive traces are formed and a bottom layer formed from compliant, low-modulus material. The bottom layer is described and illustrated throughout the Khandros patent as being a unitary layer. Figures 13 and 14, which the examiner has cited as illustrating the claimed embodiments of the present invention, merely illustrate the upper layer 838 and unitary compliant bottom layer 840 of the interposer 836. The compliant bottom layer 840 includes interspersed holes or voids 841 which, among other things, provide space into which the compliant material bulges when a test probe is put into contact with terminals 848 of the interposer 836. The remaining portion of the compliant layer 840 is referred to as "masses" 843 of low-modulus material throughout the patent. Figure 14 illustrates a cross sectional view of the structure of Figure 13. As such, although it appears in Figure 14 that a plurality of compliant masses 843 are used to adhere the interposer 836 to the semiconductor die 820, the compliant bottom layer 840 is really the same unitary layer of compliant material having holes 841 as illustrated in Figure 13, which is clearly one layer of compliant material. The space in between the masses 843 shown in Figure 14 are simply the holes 841 of the bottom layer 840.

Claim 1 is patentably distinct from the assembly described in the Khandros patent. Claim 1 recites, in pertinent part, that a plurality of pieces of adhesive film are used to adhere the semiconductor die to the interposer. As previously discussed, the Khandros patent describes a package assembly that includes an interposer having a unitary compliant bottom layer having holes interspersed throughout the layer. Nevertheless, it is still a unitary layer.

Similarly, claim 11 is patentably distinct from the method described in the Khandros patent because it recites, in pertinent part, that a semiconductor die is attached to an interposer by use of a plurality of pieces of adhesive film laminated to the interposer. Figures 13 and 14, cited by the Examiner as describing embodiments of the claimed invention, actually

show a partially sectional perspective view of the interposer 836 (Figure 13) and a cross-sectional view of the same (Figure 14). As clearly illustrated in Figure 13, and described in the related text, the compliant bottom layer 840 is a unitary and continuous layer.

For the foregoing reasons, claims 1 and 11 are patentably distinct from the assembly and method described in the Khandros patent. Consequently, the rejection of claims 1 and 11 under 35 U.S.C. 102(e) should be withdrawn.

Claims 2-7 and 9-10, which depend from claim 1, and claims 12-13 and 15-18, which depend from claim 11, are similarly patentable because of their dependency from patentable claims 1 and 11. These dependent claims further limit the claims from which they depend. For example, claim 5 recites that the plurality of pieces of adhesive film of claim 1 comprise multiple layers. Claim 18 recites that the plurality of pieces of adhesive film laminated to the interposer in claim 11 are positioned parallel along a longitude of the semiconductor die. Consequently, claims 2-7, 9-10, 12-13, and 15-18, which depend from respective patentable claims, are also patentable over the Khandros patent. Therefore, the rejection of claims 2-7, 9-10, 12-13, and 15-18 under 35 U.S.C. 102(e) should also be withdrawn.

Claims 8 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Khandros patent in light of the Examiner taking judicial notice that solder balls are commonly known in the art. However, taking judicial notice of solder balls does not make up for the deficiencies of the Khandros patent previously described. Namely, combining solder balls with the assembly described in the Khandros patent does not result in the structure or method recited in claims 8 and 14, respectively. As discussed above, Khandros describes a semiconductor package assembly including an interposer including a unitary compliant bottom layer having holes therein. Claim 8 recites a structure including a plurality of pieces of adhesive film and claim 11 recites laminating a plurality of pieces of adhesive film to an interposer to attach a semiconductor die thereto. The subject matter of claims 8 and 11 are not described in the Khandros patent.

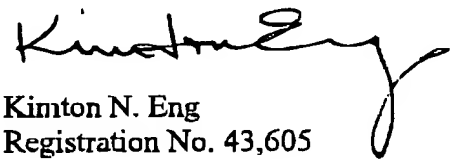
For the foregoing reasons, claims 8 and 11 are patentable over the Khandros patent in light of the Examiner taking judicial notice that solder balls are commonly known in the art. Therefore, the rejection of claims 8 and 11 under 35 U.S.C. 103(a) should be withdrawn.

Claims 38-49 have been added to claim alternative embodiments of the invention disclosed in the specification. No new matter has been added by claims 38-49.

All of the claims pending in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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